A 100-Gbit/s 2:1 Multiplexer in InP HEMT Technology

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Abstract — **In this paper, we describe a 100-Gbit/s 2:1 Multiplexer (MUX). In order to suppress the degradation of signals and to increase the operation speed, we designed interconnections for the circuit using impedance matching techniques. We fabricated the MUX with 0.13-μm InP HEMT technology, which has a cutoff frequency of 175 GHz. By using this design, we succeeded in 100-Gbit/s operation of the MUX and obtained clear eye waveforms. We also developed a V-connector module for the circuit, and achieved 80-Gbit/s operation.**

I. INTRODUCTION

The rapid growth of information technologies has created a demand for increasing the processing speed of computers and large capacities of data transmitting systems. Improving the speed of digital circuits is an effective way to raise the performance of these systems. A MUX has a role of serializing lower speed parallel data to higher such data, and some circuits have been reported in several technologies, such as SiGe HBT [1], InP HBT [2], and InP HEMT [3]. In particular, InP HEMT technology is one of the most promising because it has extremely fast electron transport characteristics. To date, a reported InP HEMT with a gate length of 25 nm has an f_T of 562 GHz [4], which shows sufficient potential for over 160-Gbit/s operation. However, at such high bit rates as over 40 Gbit/s, it is very difficult to achieve the performance because of multiple signal reflections at the interconnections and fringing capacitance of the passive components. Therefore, not only the performance of the transistors but also the design of the interconnections is key technologies to increase the operation speed of an MUX. In this paper, we describe the design of the interconnections in an MUX whose design we use to achieve 100-Gbit/s operation of the circuit.

II. TECHNOLOGY

A 0.13-μm InAlAs/InGaAs/InP HEMT technology was used to realize the circuit. The cross-sectional view of the technology is shown in figure 1. The transconductance and the cutoff frequency of the transistor are 920 mS/mm and 175 GHz, respectively. The passive components are metal-insulator-metal (MIM) capacitors made of SiN, and NiCr resistors with 50 Ω/square. Benzocyclobutene (BCB) film, which has a low relative permittivity of 2.8, is used for the inter-layer films to reduce the parasitic capacitance. Three layers of interconnections are formed using an Au-plating technique.

With this technology, the structure of interconnections and capacitors were improved from previous technology [5]. We added one more metal layer, and lifted capacitors between the 2nd and 3rd metal layers.

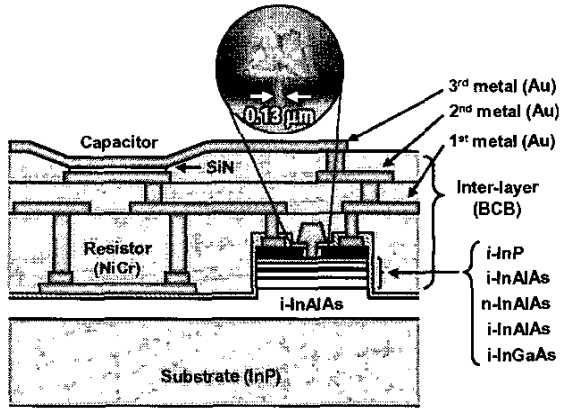

Fig. 1 Schematic cross-section of the 0.13-μm gate InP HEMT technology.

III. CIRCUIT DESIGN

Figure 2 shows a block diagram of the 2:1 MUX. Two channels input data at 50 Gbit/s are serialized at a selector by using a 50-GHz clock. Each block was designed on a source-coupled FET logic (SCFL) Because of the difficulties in aligning the phase of differential signals, we employed a single-phase input for the data and clock. To convert these signals into differential ones, buffers were placed in front of the selector. An output buffer was located in the final stage to drive the 50-Ω input load of measurement equipment.

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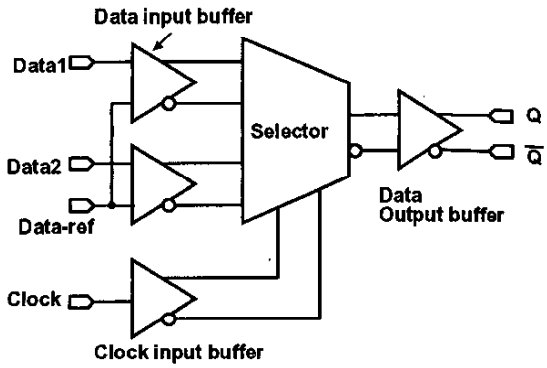

Fig. 2 Block diagram of the 2:1 MUX.

Data input buffer

A schematic diagram of the data input buffer is shown in figure 3. The buffer consists of a data input stage and three stages of an amplifier core which is composed of a source-coupled differential amplifier and a source follower. To transmit nonreturn-to-zero (NRZ) data at 50 Gbit/s, the buffer needs to have a wide bandwidth from near DC to over 40 GHz, which is 80 % of 50 GHz. The source follower is useful to convert the bias level, however, the fringing capacitance between ground lines and the electrode of speed-up capacitors make the bandwidth narrower. We've solved this problem by lifting the capacitor to the upper layer as shown in figure 1 and laying level-shift diodes under the capacitors.

Figure 4 shows the gain characteristics of a test circuit that was made for checking the performance of the data buffer. This circuit produced a bandwidth of 48 GHz and a gain of 4.3 dB at 40 GHz.

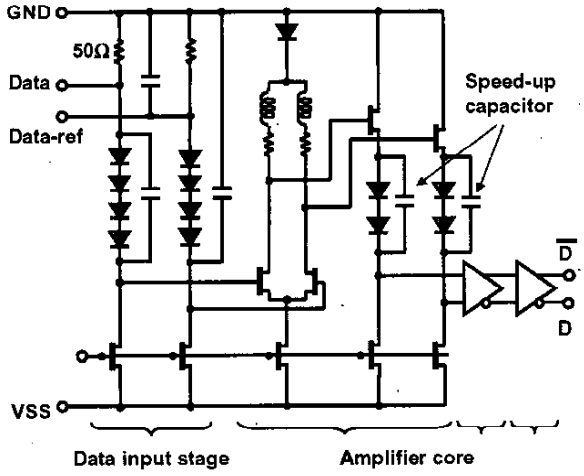

Fig. 3 Circuit schematic of the data buffer.

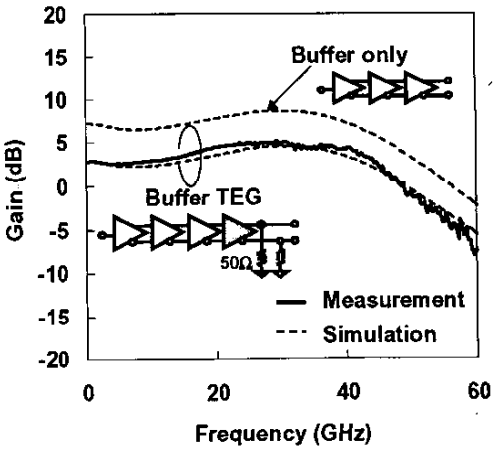

Fig. 4 Gain characteristics of the data buffer.

Since the measured result was corresponded well with the simulated one, the gain of the data input buffer is estimated to be about 7 dB at 40 GHz. The buffer has sufficient performance to transmit 50-Gbit/s data to the selector.

Selector

One of the most critical problems of high-speed digital circuits is signal reflection. At 50 GHz, a wavelength is only 2.5 mm on an InP substrate, however, since DC supply lines and other components such as capacitors extend the cell size, the length of interconnection has to be longer than one tenth of the wavelength (250 μm) and the interconnection acts as a distributed element. In general, the input impedance of common source circuits of FET is higher than 1 kΩ and does not match to the impedance of interconnection. With this connection, the output signal easily reflects at the end of the line and multiple reflections occur. In particular, the interconnections to the selector are a critical part because the selector has three signal input nodes and it is difficult to shorten the length of the interconnections. To solve these problems, we propose a design where the interconnections are extended inside a selector core.

Figure 5 shows a schematic diagram of the selector, which consists of a Gilbert cell and a source follower. During selector operation, data signals are fixed at high or low levels at data input transistors (Q_3, Q_4, Q_5 and Q_6) when the clock signals are switching at clock differential transistors (Q_1, Q_2). Therefore, Q_3, Q_4 and Q_5, Q_6 behave as a common-gate circuit, and the input impedance at the source node (A) is low compared with the impedance of a clock input node (C).

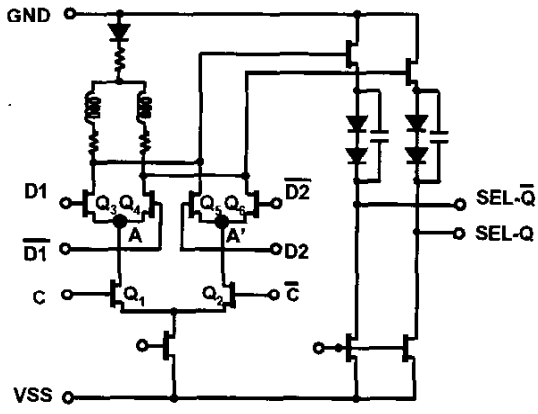

Fig. 5 Circuit schematic of the selector.

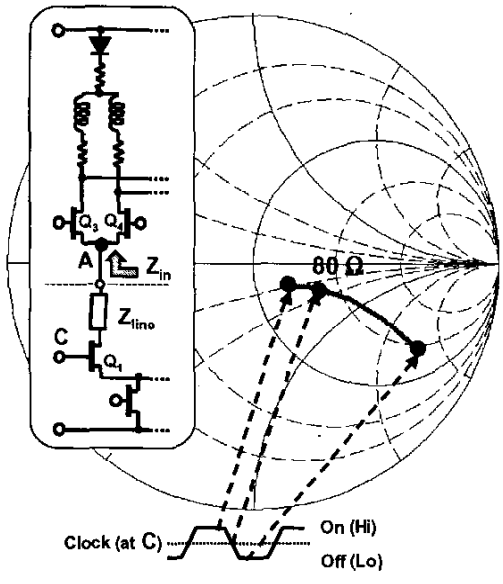

Fig. 6 Input impedance (Z_{in}) at each clock level.

Figure 6 shows input impedance (Z_{in}) at node A when the clock signals are switching. Since the impedance is low with the initial turning on of the clock (60 Ω) and at the mid-way state (80 Ω), the impedance of the interconnection (Z_{line}) can be matched.

Figure 7 shows the simulated output waveform when the line lengths were set to 300 μm, and Z_{line} was set to 30 Ω, 65 Ω and 166 Ω. Because of an impedance mismatch, the eye opening was close at 30 Ω. When Z_{line} was 166 Ω, pulse jitter increased to 1.6 ps from 0.7 ps. On the other hand, there was almost no difference between the waveforms at 65 Ω and the ideal and the increase of pulse jitter was only 0.2 ps. These results show that it is possible to extend the 65-Ω interconnection at this node without signal degradation and by using this design, we can achieve the circuit performance.

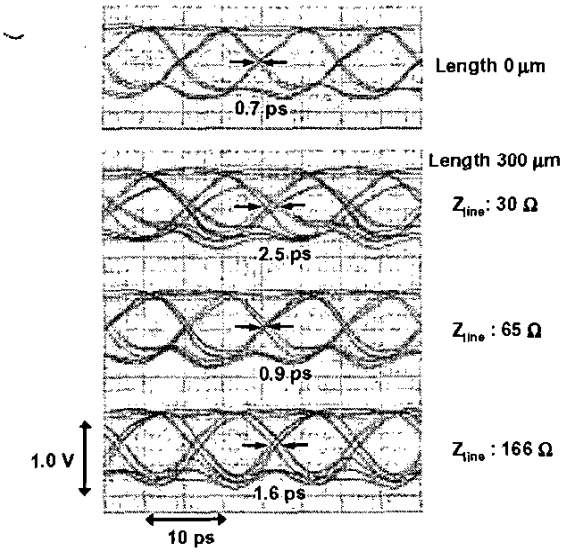

Fig. 7 Simulated output waveforms of the selector at 100 Gbit/s.

IV. EXPIRIMENTAL RESULTS

A micrograph image of the chip is shown in figure 8. The total chip area is 1.9 x 1.8 mm^2, the supply voltage is -3.3 V, and the power consumption is 1.0 W. Data signals are input from the left side and output from the right side. To reduce the offset due to the deviation of the transistors and other components, all elements of the differential circuit were designed to be completely symmetrical.

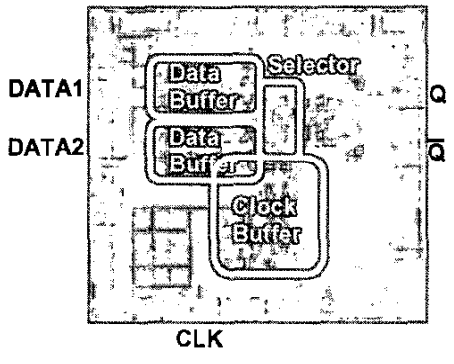

Fig. 8 Chip photograph of the 2:1MUX.

Figure 9 shows measured waveforms at 100-Gbit/s operations. The amplitude of each data was 0.75 V. Clear output waveforms have been obtained.

We also tried to mount the MUX in a module, a photograph of which is shown in figure 10. The size of the module, excluding connectors, is 30 × 30 × 9 mm. High frequency signals are drawn from a chip with coplanar waveguide (CPW) lines on a ceramic substrate, and V-connectors are used to input and output the signals. The mounted chip succeeded in making 80-Gbit/s operations, as shown in figure 11.

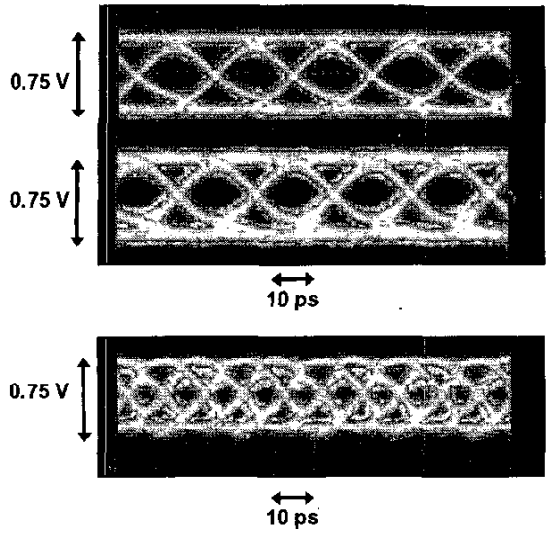

Fig. 9 Input eye diagrams at 50 Gbit/s (top: DATA1, middle: DATA2) and Output eye diagram at 100 Gbit/s (bottom).

V. Conclusion

We developed a 2:1 MUX that operate at 100 Gbit/s, which is one of the fastest operation speeds to date. By designing interconnections matching the input impedance of a circuit, we could increase operating speed and obtained high waveform quality. We also developed a V-connecter interface module, and it achieved 80-Gbit/s operations.

ACKNOWLEGMENT

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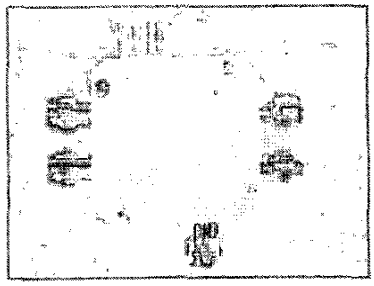

Fig. 10 Photograph of the 2:1 MUX Module.

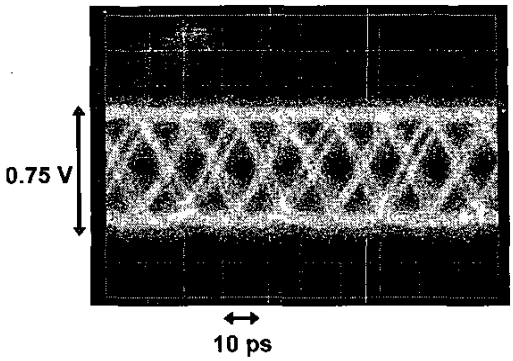

Fig. 11 Output eye diagrams of the module at 80 Gbit/s.

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